REMARKS

Favorable reconsideration of this application is respectfully requested in view of the foregoing amendments and the following remarks.

No claims have been canceled or added by this amendment. Claims 1-5, 7 and 8 have been amended. Thus, claims 1-9 remain are pending in the present application, of which claims 1 and 4 are independent.

Acknowledgement of Priority Document Receipt Requested

A certified copy of the priority document was submitted on November 20, 2003. Box 12(b) of the Office Action Summary is checked rather than box 12(a)(1). The undersigned has no reason to believe that this circumstance implies anything other than a minor oversight on the part of the USPTO. As such, it is respectfully requested that an official acknowledgement of the USPTO's receipt of the certified copy of the priority document is hereby respectfully requested.

Noted – Information Disclosure Statements Considered

The indication (see Examiner-initialed PTO form 1449s mailed with Office Action dated May 28, 2008) that the Information Disclosure Statements as filed on November 20, 2003 and December 12, 2007 and references listed therein have been considered is noted with appreciation.

Noted - Drawings Approved

The indication (see Office Action Summary, box 10(a)) that the Drawings (submitted on November 20, 2004) have been approved is noted with appreciation.

Claim Rejection Under 35 U.S.C. §102

Claims 1-9 are rejected under 35 U.S.C. §102(e) as being anticipated by Maeda et al. (U.S. Patent No. 6,618,455, hereafter Maeda).

INDEPENDENT CLAIM 1

As an example, independent claim 1 recites (among other things) a feature of "converting a first synchronous state indication code used by the first synchronization scheme into a second synchronous state indication code used by the second synchronization scheme." (Underlining is added for emphasis.) As will be explained below, at least this feature of claim 1 is a distinction over Maeda.

Maeda discloses a clock management apparatus for a synchronous network system, in which the clock signal is switched to another clock signal automatically to continue synchronous communication when the quality of a clock signal is deteriorated (Abstract). Specifically, at column 6, lines 44-48, Maeda describes that the network equipment in the synchronous network system fetches a plurality of clock signals and selectively uses a clock signal having a good quality based on the quality information of the clock signals transferred through the S1 bytes in the SOH shown in FIG. 2 or Sa4 to Sa8 bits in the SDH multiframe shown in FIG. 3. This quality information is described, for example, at column 5, lines 53-55 in which Maeda et al. indicates that quality information SSMB (synchronization status message byte) of the clock signal is transferred by using the four bits in each of the S1 bytes.

The Office Action refers to the clock signals described by Maeda at column 2, lines 5-35, and appears to equate these clock signals to the first synchronous state indication code and second synchronous state indication code recited in claim 1. However, the claimed synchronous state indication code is not a clock signal, but is a code indicative of synchronous state as to the quality of a timing source. The characterization of the claimed synchronous state indication code as equivalent to a clock signal is thus improper.

Even if it is agreed, for the sake of argument, that the claimed synchronous state indication code can properly be equated to a clock signal, all that Maeda discloses is the switching of clock signals from the use of one clock signal to the use of another clock signal. Nowhere does Maeda disclose or suggest converting a clock

signal to another clock signal. Further, Maeda is silent about the conversion of the quality information transferred through the S1 bytes in the SOH shown in FIG. 2 or Sa4 to Sa8 bits in the SDH multiframe shown in FIG. 3. At most, Maeda discloses the use of the quality information to determine whether the clock signal being used has good quality. Hence, the noted feature, namely "converting a first synchronous state indication code used by the first synchronization scheme into a second synchronous state indication code used by the second synchronization scheme," is a distinction over Maeda. (Underlining is added for emphasis.)

Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. In view of the distinction of claim 1 noted above, at least one claimed element is not present in Maeda. Hence, Maeda does not anticipate claim 1.

Amended independent claim 4 recites (among other things) a feature similar to the above-noted feature of independent claim 1. As such, Maeda fails to anticipate claim 4 based at least on the feature of claim 4 that is similar to the above- noted feature of independent claim 1.

Claims 2-3 and 5-9 ultimately depend from one of independent claims 1 and 4, and so at least similarly distinguish over Maeda. Hence, Maeda also does not anticipate claims 2-3 and 5-9.

Conclusion

In light of the foregoing, withdrawal of the rejections of record and allowance of this application are earnestly solicited.

Should the Examiner believe that a telephone conference with the undersigned would assist in resolving any issues pertaining to the allowability of the above-identified application, please contact the undersigned at the telephone number listed below. Please grant any required extensions of time and charge any fees due in connection with this request to deposit account no. 50-4610.

Respectfully submitted,

Dated: September 29, 2008

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